REMARKS

In the Office Action mailed December 10, 2004, the Examiner rejected claims 1-6, 15, 19-22, 24, 26 and 28 under 35 U.S.C. § 102(b) as being anticipated by or, in the alternative, under 35 USC 103(a) as obvious over Nemati et al. The Examiner also required submission of formal drawings. In the present response, claims 1, 6, 15, 19 and 22-24 have been amended and claim 28 cancelled. Formal drawings are also submitted. Reconsideration of the present application in view of the above amendment and the following remarks is respectfully requested.

Rejection of Independent Claims 1, 6, and 19:

Claims 1 and 6 are amended to recite that the control port is configured and arranged to receive a second signal that is generated outside of the thyristor. This second signal is coupled to at least the second base region by the second control port to control the holding current or forward blockage voltage of the thyristor. Claim 19 is amended to recite that the signal is generated outside of the thyristor and is coupled to at least one of the base regions for controlling the holding current or forward block voltage as a function of temperature. On the other hand, Nemati discloses "a shunt between a base and emitter region in a thyristor that effects a leakage current **in the thyristor**" and "the current shunt is configured and arranged to shunt low-level current **between** the emitter region and the adjacent base region" (see abstract of Nemati, emphasis added). The current in Nemati is generated by the thyristor. The "shunt" of Nemati is different from the claimed control port. More specific details of the differences between Nemati and the present invention are described below.

In the office action, the Examiner refers to Fig. 5a of Nemati to support the rejection. Nemati describes Fig. 5a as follows (col. 6, lines 31-45; emphasis added):

> "FIG. 5a shows another example embodiment of the present invention, wherein a tunnel node 542 and tunnel dielectric 544 are formed over the base 514 of an anode end portion 510 of a capacitively coupled thyristor 500. The tunnel node is resistively coupled to the base 514 via a tunneling current through the tunnel

dielectric, which is sufficiently small in thickness (in one example implementation, about 30 angstroms) **to permit leakage current from the base to the tunnel node**. As with other examples described hereinabove, the thyristor includes gate 530 capacitively coupled to a base region 524 of a cathode end portion 520 of the thyristor, which also includes emitter region 522 and, at the anode end portion 510, an emitter region 512."

It can be seen from the above quoted paragraph that the function of the tunnel node is to permit leakage current from the base to the tunnel node. On the other hand, claims 1, 6 and 19 recite that the control port couples to a base region a signal generated outside of the thyristor. Thus, there are significant differences between Fig. 5a and the claim invention.

The Examiner also refers to Fig. 8. Nemati describes Fig. 8 as follows (col. 7, lines 17-39; emphasis added):

"FIG. 8 shows another example embodiment of the present invention in which **an NMOSFET 850 is used to provide a current shunt between anode 812 and n-base 814 of a capacitively-coupled thyristor 800.** The source, drain and gate of the NMOSFET are electrically connected to the anode, n-base, and p-base of the thyristor, respectively, when the thyristor is in the forward conducting state, the voltage difference between the gate and source of the NMOSFET is relatively small (such as 0.1V to 0.2V). Therefore, the NMOSFET passes only a very small current and the holding current of the thyristor is acceptably low. When the thyristor is in the forward blocking state, the voltage difference between the gate and source of the NMOSFET is very high (almost equal to the anode to cathode voltage of the thyristor) and the NMOSFET has a small resistance. This approach provides a strong shunt between the anode and n-base of the thyristor, and provides high stability for the blocking state of the thyristor against high temperature and disturbances. Alternatively, the gate of the NMOSFET can be independently controlled rather than being connected to the p-base. Other embodiments regarding the use of a FET in combination with a thyristor can be found in U.S. Pat. No. 4,323,793, which is fully incorporated herein by reference."

In Nemati, the function of the NMOSFET and the tunnel node is to shunt current in the thyristor. On the other hand, claims 1, 6 and 19 recite that the control port couples to a base region a signal generated outside of the thyristor. Again, there are significant differences between Fig. 8 and the claim invention.

Not only is the present invention not anticipated by Nemati, it is also not rendered obvious. It is nonobvious to change from shunting current in the thyristor (as disclosed in Nemati) to applying an externally generated signal to the thyristor. Further, Nemati does not suggest that the externally generated signal needs to "control holding current or forward blocking voltage of the thyristor as a function of temperature" (claim 1), or "as a function of the detected failure for controlling holding current or forward blocking voltage of the thyristor" (claim 6), or "controlling the holding current or forward blocking voltage as a function of temperature" (claim 19).

In view of the significant differences between Nemati and claims 1, 6 and 19, these claims are patentable over Nemati.

Rejection of Claims 2-5:

Claims 2-5 recites additional limitations related to the second signal. Because Nemati does not teach or suggest the "second signal," there is even less motivation to add limitations in claims 2-5 to Nemati. Consequently, these claims are patentable over Nemati.

Rejection of Claim 15:

Claim 15 recites: "The memory device of claim 6, wherein the second control port and the second base region are configured and arranged such that the second signal increases carrier depletion in the second base region." The Examiner stated that "Claim 15 is rejected as the magnitude of the "signal" or voltage to the n-base at least partly determines the depletion in the n-base." Nemati does not teach or suggest applying an externally generated signal or voltage to the base region. Further, claim 15 recites a specific relationship between the second signal and the carrier depletion. This is not taught or rendered obvious by Nemati. Consequently, claim 15 is patentable over Nemati.

Rejection of Claims 24 and 26:

Claims 24 and 26 recite that one of the base regions includes material having defects in a depletion region facing the second control port. The Examiner states that claims 24 and 26 are rejected as Fig. 7 of Nemati shows low-lifetime region. Fig. 7 of Nemati relates to minority carrier lifetime in a base-emitter depletion region as means for providing low level shunting leakage current. There is no teaching or suggestion to form a second control port on top of this region. As discussed above in connection with claims 1, 6 and 19, the tunnel node and NMOSFET in Nemati are different than the control port in claims 1, 6 and 19. Thus, even if the tunnel node and NMOSFET are placed on top of the depletion region, the new device will operate differently than the claim invention. Consequently, claims 24 and 26 are patentable over Nemati.

Rejection of Claims 20-22:

These claims depend from independent claims 1, 6 and 19. They are patentable over Nemati on at least the same basis as the corresponding independent claims.

Drawings:

Formal drawings are included in this response.

Others:

A PTO-1449 is submitted together with the present amendment. The Examiner is invited to consider the references listed therein.

It is believed that all grounds of rejection have been satisfactorily answered. The allowance of the present application is respectfully urged.

The Commissioner is authorized to charge any fee for this filing to Deposit Account 50-2538 (docket number C-028).

Respectfully Submitted

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